25.2 A 10b 160MS/s 84mW 1V Subranging ADC in 90nm CMOS

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High-speed low-power ADCs are critical components of mixed-signal SoCs. When cost is of primary importance, these embedded ADCs are required to have low area and to be compatible with the low supply voltage utilized by digital CMOS. Furthermore, the circuit architecture should scale well to future technology nodes so as to minimize design effort in the event of a process shrink. Subranging ADCs can meet these requirements well. The highly regular structure of their key components simplifies layout and helps achieve low area. Due to their use of low-gain open-loop amplifier stages, they perform well at low voltage and are insensitive to low intrinsic transistor gain, making them highly scalable. In this paper, a 10b 160MS/s subranging ADC that consumes 84mW from a single 1V supply is presented. The ADC occupies 0.42mm^2 in a fully digital 90nm CMOS process. The prototype ADC achieves >9.1 ENOB and 75dB SFDR across the full Nyquist band, and retains 8.5 ENOB and 70dB SFDR to 200MHz.

The proposed 2-step subranging ADC, shown in Fig. 25.2.1, comprises a THA, a 5b coarse flash ADC (CADC), a 6b fine flash ADC (FADC), coarse/fine resistor ladders, and fine reference MUX. Although power-hungry and not as scalable as the subranging core, the THA is necessary in this design to meet the target SFDR at Nyquist. By sampling the input precisely and presenting a static voltage to the CADC and FADC, the THA mitigates timing skews in the sub- converters that would otherwise cause distortion at high frequency. If the ADC input is already discrete-time, if the ADC bandwidth is small, or if more distortion is acceptable, then the THA can be eliminated. In this design, the CADC and FADC sampling switches are clocked on opposite clock phases, which increases FADC latency by 1/2 clock period and gives the CADC time to perform the coarse quantization [1]. Designs without a THA must sample CADC and FADC inputs simultaneously, but can implement the required latency by interleaving 2 sets of FADC input capacitors [2]. One bit of overrange in the FADC corrects for CADC offsets up to 1/ 2 subrange (i.e. 16LSB).

The THA consists of an OTA, switches, and sampling capacitors in the conventional flip-around configuration. The input switches are bootstrapped for high tracking bandwidth and linearity. A 2-stage OTA topology, shown in Fig. 25.2.2, is chosen in order to maximize output swing. Although efficiency is poor compared to a single-stage OTA, the large swing allows the use of smaller capacitors in the noise-limited FADC and results in lower system power than using a more efficient OTA with less swing. An SC level-shift circuit allows the use of a class-A-biased inverter for the 2nd stage, which yields twice the transconductance of a conventional common-source stage at the same bias current. Gain-boosting in the first stage helps to suppress nonlinearity that results from compression at high swing. The final design achieves 74dB DC gain, 1GHz unity-gain bandwidth, and 75dB SFDR at 1.5V$_{pp}$ output swing while consuming 34mW from a 1V supply.

The CADC uses 32 identical preamplifer/comparator slices to generate the 5b coarse ADC code. Each slice consists of a 2-stage autozeroed preamplifier and a comparator. In order to provide more time for fine ladder settling, the CADC comparators are latched before the THA output is completely settled, absorbing some of the over-range allowance. The comparator offset is < ±50mV, and approximately ±4mV when input referred, including contributions from the preamplifiers and switch charge injection. The CADC, including drivers for the RDAC MUX select lines, consumes 6mW, and occupies 0.055mm^2.

The FADC requires reference voltages from 1 of 32 subranges to generate the fine ADC code. Thus, each FADC input requires a 32:1 analog MUX. The large fanout of the MUX switches, coupled with the wide swing of the reference signal, presents a potential bottleneck to the speed of the converter. Typically, transmission gates are used for switches that must pass signals with rail-to-rail swing. However, at low supply voltage in 90nm CMOS, transmission gates have poor conductance near mid-supply. At V_{DD}=1.0V on the SS corner, degradation of t-gate conductance at mid-supply can be as high as 70%. To alleviate this problem, bootstrapped switches are used in the MUX to pass references for the middle sub-ranges. NMOS-only and PMOS-only switches are used for the high and low subranges, respectively. The differential references are obtained from 2 resistor ladders that consume a total of 12mW. Including MUX switches, the RDAC occupies 0.04mm^2. CADC references are generated by separate ladders that consume an additional 3mW.

The absence of a residue amplifier in this subranging converter places stringent offset and noise requirements on the FADC, which are overcome at modest power dissipation through the use of autozeroing and averaging. The FADC architecture, shown in Fig. 25.2.3, comprises a 3-stage autozeroed preamp array driving autozeroed comparators. Output offset storage (OOS) techniques are used exclusively throughout the FADC to provide large offset suppression without high-gain stages. The preamp uses resistive averaging at the output of the 1st and 3rd stages to reduce kT/C noise from autozeroing capacitors C1 and C3 by a factor of 4 and 16, respectively. The resulting smaller capacitors not only reduce FADC power, but also the THA load and thus the THA power. Autozeroing capacitors also serve to pipeline the preamp gain, which avoids placing excessive bandwidth requirements on preamp stages. 4× interpolation in the first stage reduces MUX complexity and increases layout pitch to allow the use of linear metal capacitors for C1, which avoids nonlinear THA settling; C2 and C3 are implemented as MOS varactors for high density. The autozeroed comparator eliminates the need for large preamp gain, reducing the number of preamp stages and the preamp power dissipation. The comparator comprises a pair of transconductors driving a common resistive load and an OOS capacitor [3]. Comparator power consumption is 170µW and residual offset is simulated to be 800µV. Total FADC power consumption is 28mW.

The prototype ADC is implemented in a fully digital 90nm CMOS GP process with no analog options. Figure 25.2.4 shows the performance of the prototype as a function of sample rate, input frequency, and supply voltage. At 160MS/s and 1.0V supply, the ENOB is 9.2b for 10MHz, 9.1b for 80MHz, and 8.5b for 200MHz; SFDR is better than 75dB to 80MHz and better than 70dB to 200MHz. A sample output spectrum at 160MS/s and 78MHz input is shown in Fig. 25.2.5. Converter performance is summarized in Fig. 25.2.6. Power consumption at 160MS/s and 1.0V supply is 84mW, excluding the digital output buffers. FOM, defined as Power/(fs*2^{ENOB}), is 0.89pJ/conv. The active die area is 0.42mm^2; the layout is shown in Fig. 25.2.7.

References:

[1] J. Mulder, C.M. Ward, Lin Chi-Hung, et al., "A 21-mW 8-b 125-MSample/s ADC in 0.09-mm^2 0.13-µm CMOS," *IEEE J. Solid-State Circuits*, vol 39, pp. 2116-2125, Dec., 2004

[2] Y. Shimizu, S. Murayama, Kohhei Kudoh, et al., "A 30mW 12b 40MS/s Subranging ADC with a High-Gain Offset- Canceling Positive-Feedback Amplifier in 90nm Digital CMOS," *ISSCC Dig. Tech. Papers*, pp. 216-217, Feb., 2006

[3] B. Razavi and B. Wooley, "Design Techniques for High-Speed, High-Resolution Comparators," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1916-1926, Dec., 1992.

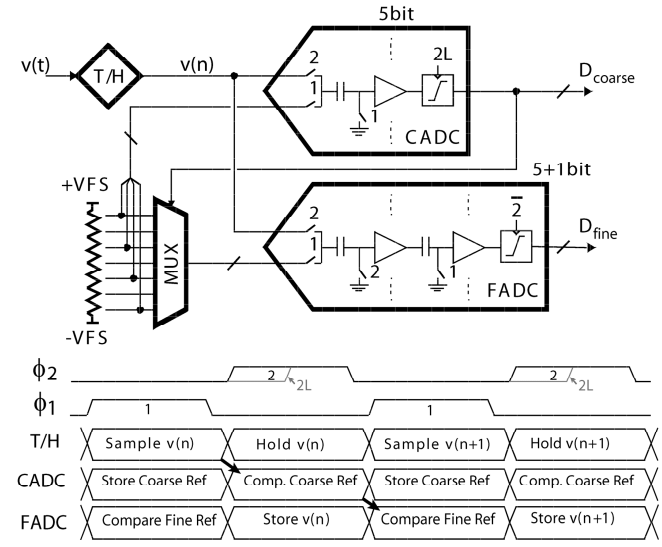
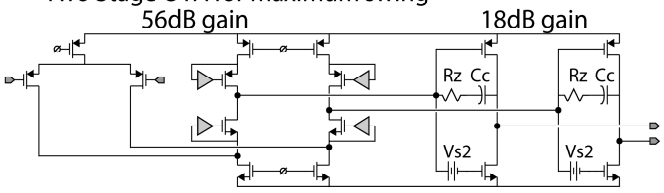
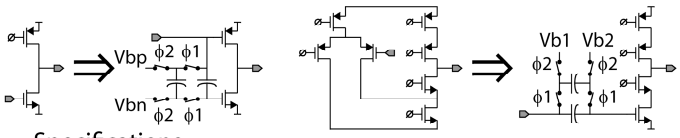


Figure 25.2.1: Subranging ADC block diagram.

- Two Stage OTA for maximum swing



- Inverter 2nd stage gives 2x current efficiency
- SC level shift used in 2nd stage and boost amps



- Specifications

  Bias Current 34mA, Input Capacitance: 150fF, DC Gain: 74dB
  UGB: 1GHz, PM: 70d (3pF load), Swing 1.5Vpp

Figure 25.2.2: THA OTA schematic.

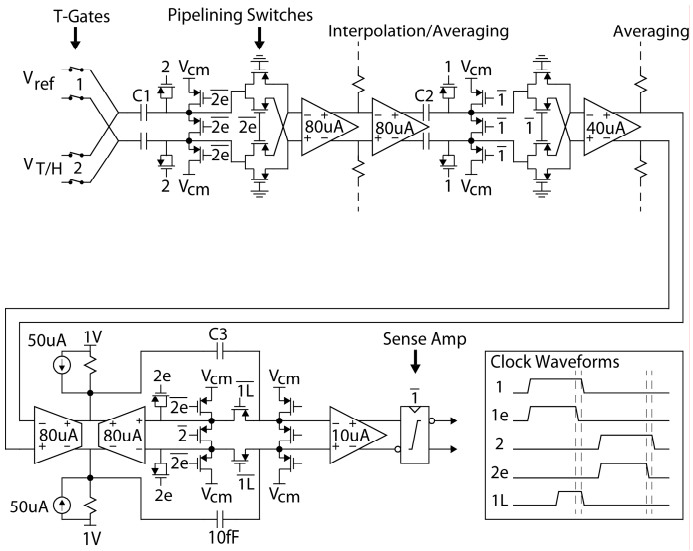


Figure 25.2.3: FADC schematic.

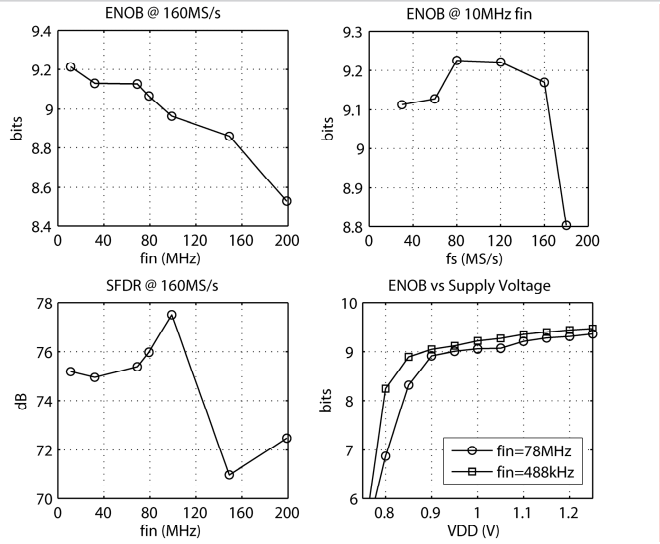


Figure 25.2.4: Performance as a function of sample rate, frequency, and supply voltage.

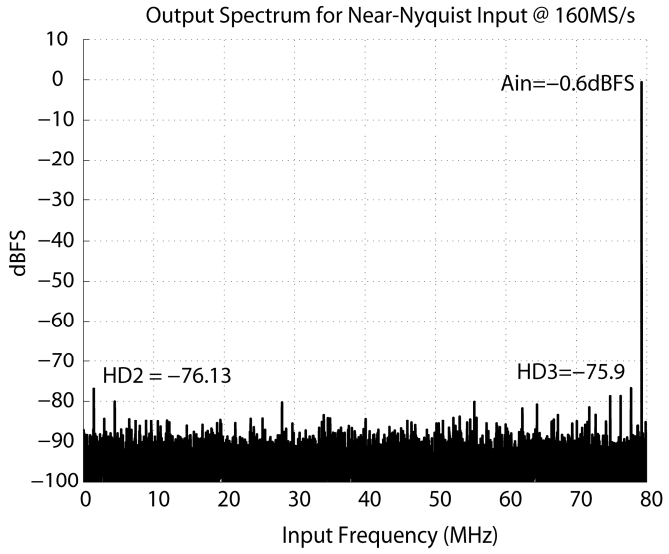


Figure 25.2.5: Sample output spectrum.

Resolution	10b
Sample Rate	160MS/s
Process	90nm GP CMOS
Supply Voltage	1.0V
Area	1.0×0.42mm^2
ENOB	9.2b
SFDR	75dB
FOM	0.89pJ/conv
Total Power	84mW
THA Power	34mW
FADC Power	28mW
CADC Power	6mW
Ladder Power	15mW
Digital Power	1mW

Figure 25.2.6: Performance summary.

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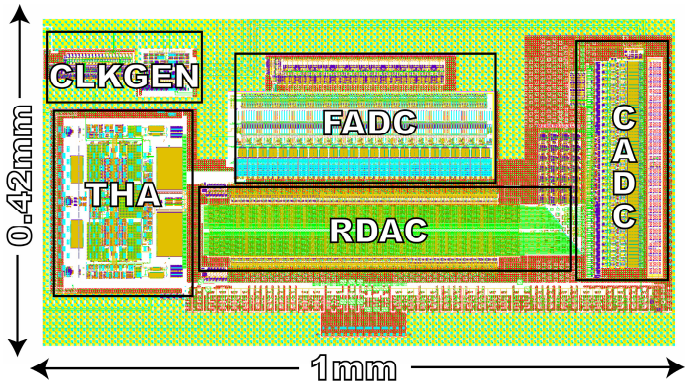

Figure 25.2.7: ADC layout.

